Docket No. 0756-1896

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	Art Unit: 2814
Hisashi OHTANI et al.	)	Examiner: P. Cao
Serial No. 09/197,767	)	
Filed: November 23, 1998	)	
For: SEMICONDUCTOR DEVICE	)	
AND PROCESS FOR	)	
PRODUCING THE SAME	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with The United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on 5-2-2003

Linda M. Hampe

PRELIMINARY RESPONSE

Honorable Commissioner of Patents
Washington, D.C. 20231

Sir:

The Official Action mailed January 2, 2003 has been received and its contents carefully noted. Filed concurrently herewith are an *RCE* and *Request for One Month Extension of Time* which extends the shortened statutory period for response to May 2, 2003. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicants note with appreciation the consideration of the Information Disclosure Statements filed on March 16, 2000; June 14, 2000; October 19, 2000; January 31, 2001; October 31, 2001; February 28, 2002, and June 13, 2002. A further Information Disclosure Statement is submitted herewith and careful review and consideration of this Information Disclosure Statement is requested.

Claims 1-6, 9, 10, 15, 16, 22-27, 40 and 46-74 are pending in the present application, of which claims 1-6 and 48-50 are independent. For the reasons set forth in detail below, these claims are believed to be in condition for allowance.

Paragraphs 2-7 of the Official Action reject claims 1-5, 16, 22-27, 40 and 46-74 as obvious based on U.S. Patent 6,081,305 to Sato et al. in view of one or more of the following patents: U.S. Patent 5,706,064 to Fukunaga et al., U.S. Patent 5,990,542 to Yamazaki, and U.S. Patent 6,097,453 to Okita. The Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Specifically, Sato does not teach or suggest a semiconductor device with both a pixel electrode and an embedded conductive layer provided to fill a contact hole with a top surface flush with a top surface of an interlayer insulating film. The Official Action asserts that Fig. 2 of Sato discloses an embedded conductive layer 171. As previously stressed, the Applicants respectfully disagree. Reference number 171 in Sato refers to a through hole (col. 15, line 4) and not an embedded conductive layer. Sato discloses a third metal layer 180 formed on the third insulating layer 170 which penetrates the insulating layer 170 to contact the second metal layer 160 (col. 14, lines 19-21). As such, the third metal layer 180 of Sato includes the portion which fills the through hole 171. Therefore, Sato does not teach a semiconductor device comprising both a pixel electrode and an embedded conductive layer but rather merely teaches a single element (third metal layer 180) that forms the pixel electrode 181 and fills the through hole 171.

Paragraph 10 of the Official Action, response to arguments, the Official Action asserts that the drawings of Sato must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art. The Official Action further states that it does not matter that the feature shown is unintended or unexplained in the specification. The reference, however, must be considered for what it teaches as a whole. Sato is not silent about elements 171, 180 and 181. Rather, Sato makes clear that element 171 is a hole and that third metal layer 180 penetrates the insulating layer 170 to contact the second metal layer 160. Thus, when taken together for what they teach as a whole, the drawings and specification of Sato would not suggest to one of skill in the art to form a semiconductor device with both a pixel electrode and an embedded conductive layer provided to fill a contact hole with a top surface flush with a top surface of an interlayer insulating film.

Furthermore, Fukunaga, Yamazaki and Okita do not cure the deficiencies in Sato. Nothing in the prior art, either alone or in combination, suggests dividing the third metal layer 180 of Sato into a reflective pixel electrode and an embedded conductive layer provided to fill a contact hole with a top surface flush with a top surface of an interlayer insulating film.

Accordingly, reconsideration and withdrawal of the rejection of claims 1-5, 16, 22-27, 40 and 46-74 under 35 U.S.C. § 103(a) is in order and respectfully requested.

Paragraphs 8 and 9 of the Official Action reject claims 6 and 15 as obvious based on the combination of Yamazaki and U.S. Patent 5,948,705 to Jun, and claims 9 and 10 as obvious based on the combination of Yamazaki, Jun and Fukunaga. The Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

There is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Yamazaki and Jun or to combine reference teachings to achieve the claimed invention. Specifically, the Applicants respectfully submit that there is no teaching in the prior art to teach or suggest how the interconnection line of Jun would be used in lieu of the pixel electrode of Yamazaki.

The Applicants further contend that even assuming, *arguendo*, that the combination of Yamazaki and Jun is proper; there is a lack of suggestion as to why a skilled artisan would use the proposed modifications to achieve the unobvious advantages first recognized by the Applicants. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

Accordingly, reconsideration and withdrawal of the rejection of claims 6, 9, 10 and 15 under 35 U.S.C. § 103(a) is in order and respectfully requested.

Finally, with the filing of this RCE, Applicants request a personal interview with the Examiner to further clarify the distinctions between the present invention and the cited prior art. It is requested the Examiner contact the undersigned upon receipt of this Response to schedule such interview.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789